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Open Hardware Technology Commons

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Antonino Tumeo
NIST RFI response contributors
SODA “Drinkers”

U.S. DEPARTMENT OF ENERGY BATTELLE

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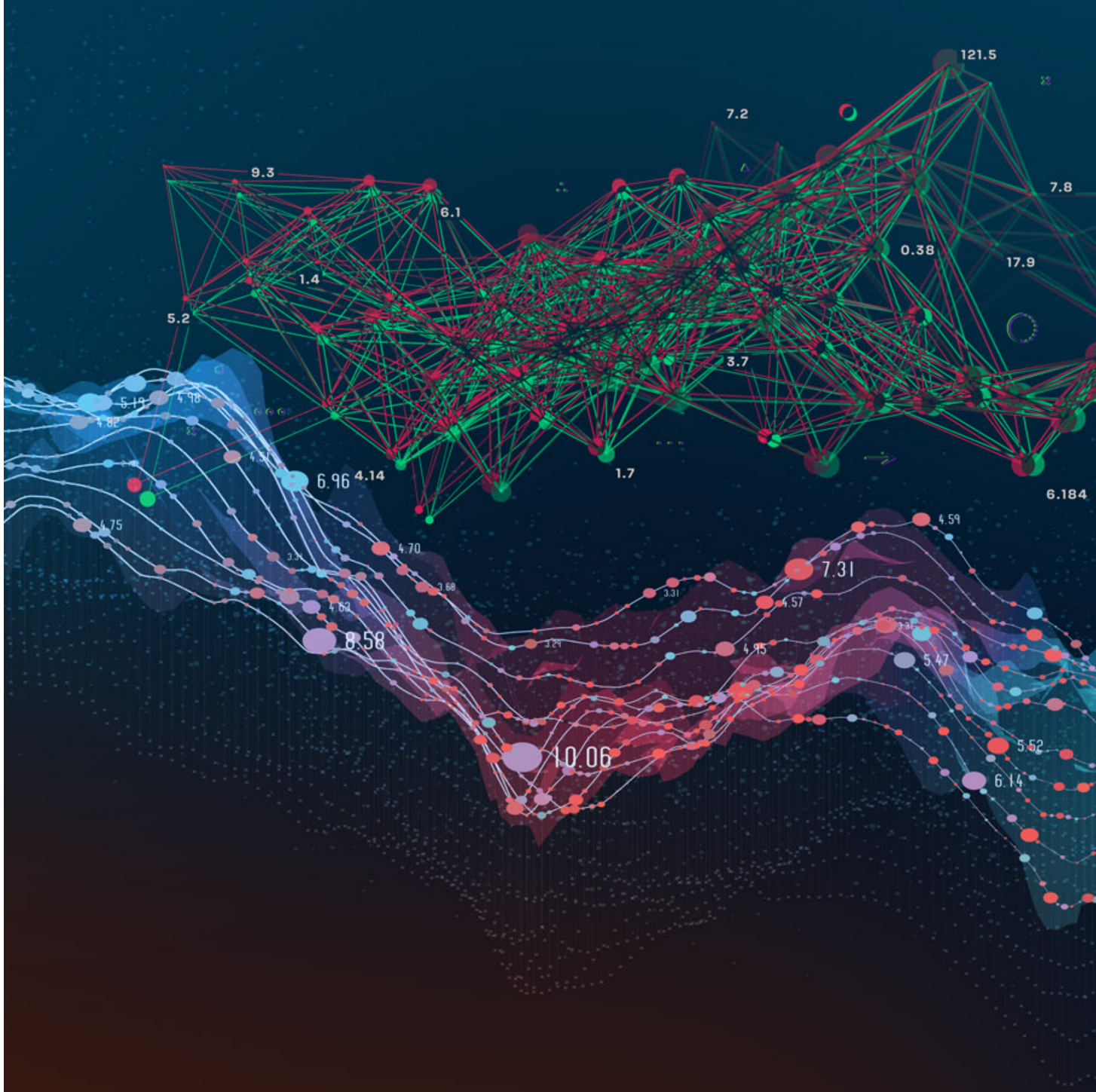

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The National Semiconductor Technology Center

Planning for NSTC – Capabilities and Structure

NIST

Capabilities Provided by NSTC

- Design infrastructure, including
  - access to circuit design/architectures, and computer automated design tools; and
  - access to established circuit design libraries;
- Fabrication of prototype integrated circuits at the leading-edge;
- Prototyping of new gate stacks and interconnect materials, processes, and structures;
- Instrumentation for materials characterization, metrology, processing, and testing of next generation, prototype devices, interconnects, circuits, and systems;
- Support for multi-project wafer runs (including fab access, integrated design tools, etc.) to enable research of new circuit architectures and structures, and small-volume prototyping;
- Fabrication for integration of functionalities that do not necessarily scale like historical transistor designs ("More than Moore");
- Prototyping of new computing architectures, including those incorporating non-silicon processes (which may require partnership or affiliation with other institutions); and
- Packaging and test; heterogeneous integration; modeling, design and simulation (in coordination with the Advanced Packaging Program to be established by NIST).

Potential NSTC Models

Centralized Facility

Mix of Centralized and Distributed Capabilities

Fully Distributed

14

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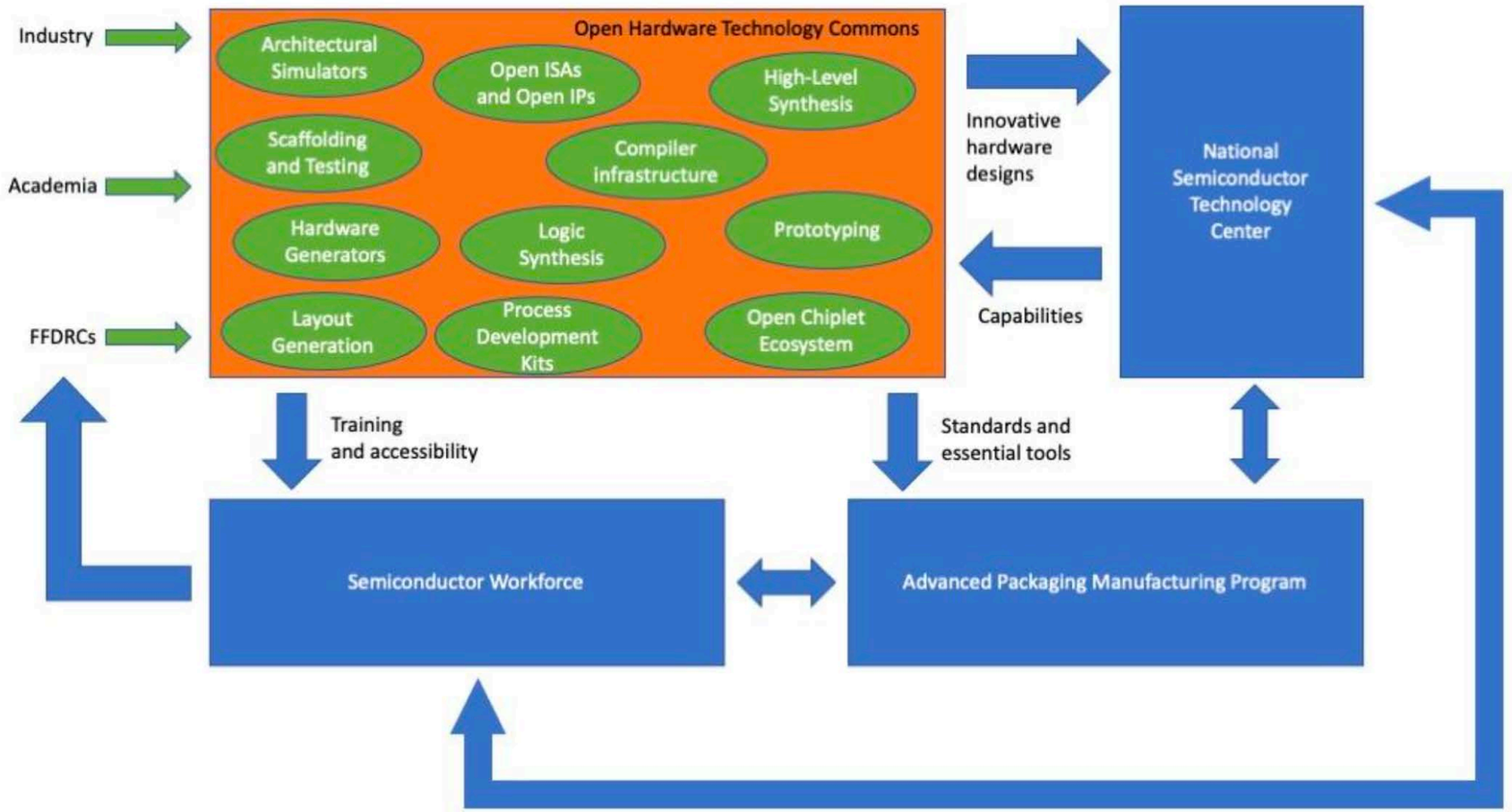

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The Vision

- Open and extensible portfolio of composable and interoperable hardware, software, design automation, and architecture design tools
  - Interoperability at all levels, with support to proprietary tools
  - Rapid prototyping of new computing concepts, quantifying their impact
- A key step in bridging the “valley of death” between Research & Development of advanced computing concepts and the late-stage product development that is the provenance of industry
  - Needed for an NSTC on-ramp
  - Unlocks barrier to innovation
  - If access to the NSTC is limited to traditional closed hardware design ecosystems, the high barriers to entry will limit participation to only a few privileged organizations that can access and wield hardware design tools.

Conclusions

- We are already starting to see integration and extendibility
  - Community has been already working to enable the OHTC concepts
- The NSTC is a unique opportunity to move our tools to the next step
  - NSTC key focus is leading edge technology
  - Many open-source tools are specifically born to support exploration of advanced concepts
  - The ensemble of the tools and technology will be bigger than the sum of the components, we can move towards tools that are not only research vehicles but are regularly exercised for advanced development
- Lower barriers of entry, train next generation of the workforce

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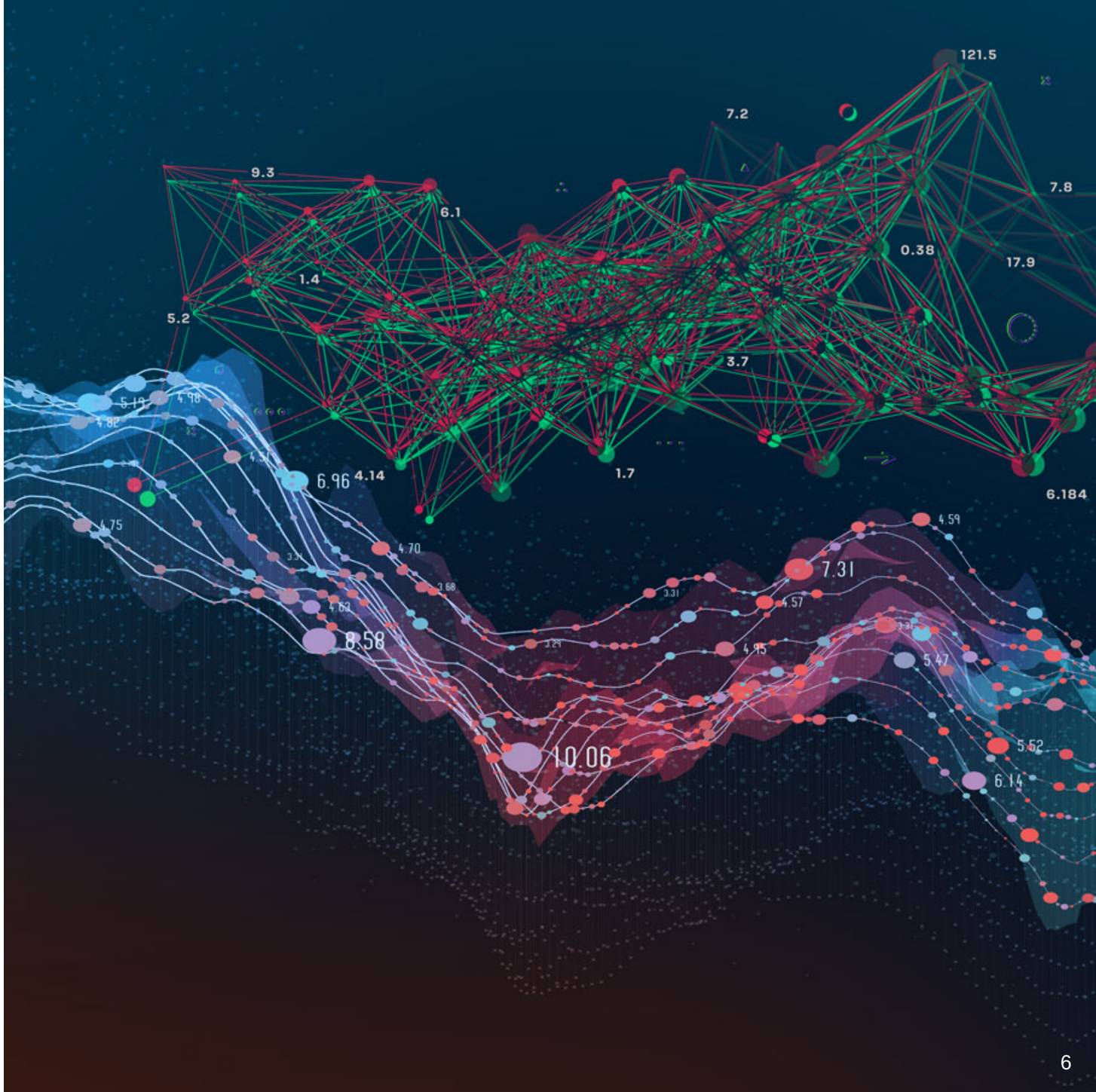
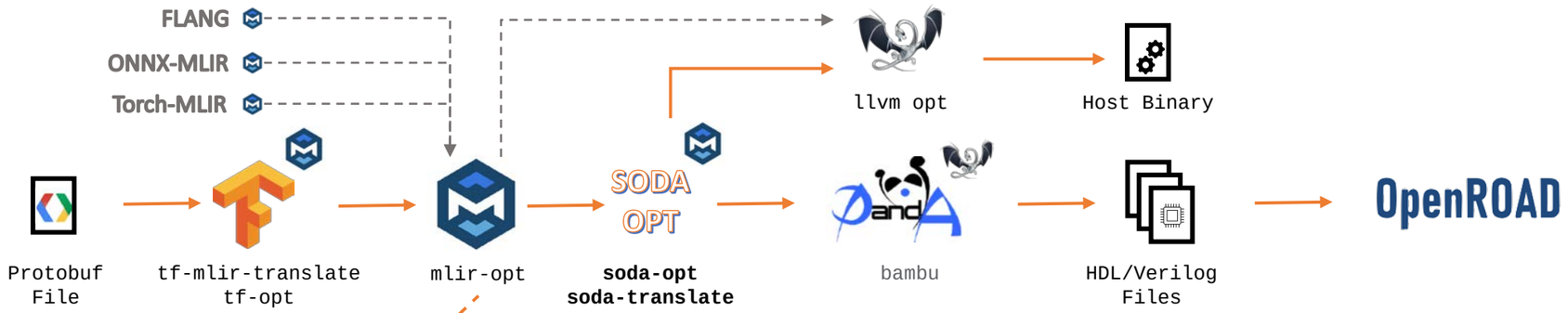
Thank you



Practical Example: SODA Synthesizer



TF-OPT:

- Domain Specific (DNN) optimizations

MLIR-OPT:

- Progressive lowering
- Provides “MLIR IR”

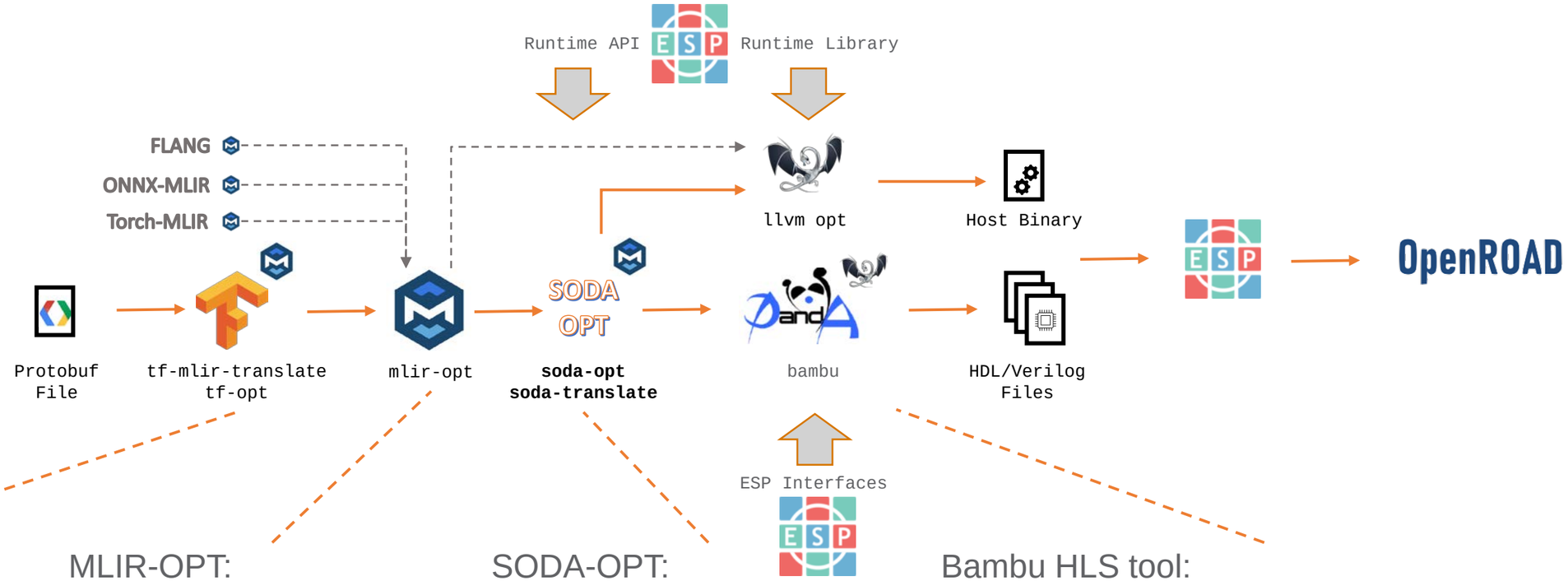
SODA-OPT:

- Software partitioning
- High-Level optimizations
- Code preparation for HLS
- Host code generation

Bambu HLS tool:

- Allocation of hardware modules
- Scheduling of operations
- Binding operations to allocated modules
- HDL code generation for different targets (FPGA or ASIC)

Practical Example: SODA Synthesizer + Prototyping Platform



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Another Practical Example

- PandA-Bambu as a frontend for Silicon Compiler
- PandA-Bambu backends for FPGAs and ASIC
  - FPGAs: Vendor Independent and can target OpenFPGA
  - ASICs: Tested with both open-source and proprietary tools